HIGH PERFORMANCE MONOLITHIC POWER AMPLIFIER USING A UNIQUE ION IMPLANTATION PROCESS

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ABSTRACT

State-of-the-art X-band power FETs and monolithic amplifiers have been fabricated by a high yield planar process using a unique double-peaked implant profile. A 1-mm FET has achieved 40 percent power added efficiency with 720 mW output power and 6.3 dB gain at 10 GHz. A two-stage monolithic amplifier has delivered 2.2 W output power at 9.5 GHz for a record 0.6 W/mm power density. The monolithic amplifier chips have also achieved 20 percent dc-yield and 5 percent uniformity in I_{DSS} and V_{PO}.

INTRODUCTION

Recent advances in GaAs material and device technology have resulted in excellent performance of GaAs power FETs and monolithic amplifiers[1]. The FET active layers can be formed by VPE,[2],[3] MBE,[4],[5] or ion implantation.[6],[7],[8] While VPE and MBE materials generally produce devices with better power performance due to their ability in forming heavy N^+ layer and sharp doping profile, they are less desirable for high volume MMIC production because of their higher cost and lower uniformity/reproducibility. Ion implantation technology, in contrast, is ideal for monolithic circuits because of its flexibility in fabricating planar structures and integrating different devices on the same chip, as well as its better uniformity /reproducibility, higher throughput and lower cost. However, power devices fabricated on ion-implanted materials have shown generally lower power performance. This paper describes results achieved with a unique ion implantation process that has produced X-band power FETs and two-stage monolithic amplifiers showing state-of-the-art performance.

FABRICATION OF ION IMPLANTED POWER FETs

The fabrication procedure is similar to that reported in reference (9), except for the active layer formation by a planar, double ion-implantation process.

The key to fabricating FETs with high power and high efficiency is to maximize the drain voltage capability while maintaining a high channel current. There are two failure mechanisms that limit the maximum drain voltage -- the drain-gate breakdown and the drain-source burnout. The drain-gate breakdown is caused by avalanche of the Schottky gate, which starts at the maximum electric field region near the gate edge on the drain side. The field distribution near the gate is strongly influenced by the doping concentration, channel thickness and topology of the gate recess. the other failure mechanism that limits the drain voltage is the drain burnout. Because of the high current density (current crowding) at the drain edge, catastrophic failure usually occurs when high drain voltage causes the local temperature to reach the GaAs decomposition point.

We have developed an optimum double-peaked implant profile which is able to significantly increase the FET's drain voltage capability and power performance. The doping profile, as shown in Figure 1, is formed by a double-energy Si-implantation in an undoped LEC GaAs substrate, followed by a 890°C capless anneal. The high surface concentration (N_D = 4-5 x 10^{17} cm^{-3}) allows for low source and drain resistances and high drain burnout voltage, whereas the second peak (N_D = 1.5 x 10^{17} cm^{-3}) carries the necessary channel current for a typical power FET. A 1000 Å channel recess is etched in the gate area so the Schottky gate can be placed at the low concentration region between the peaks to enhance the gate-drain breakdown voltage.

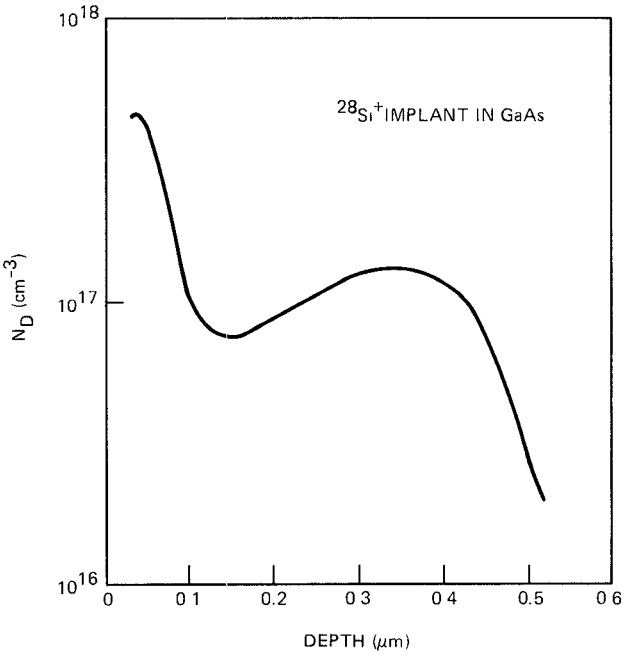

Figure 1 Optimum double-peaked implant profile for X-band power FET.

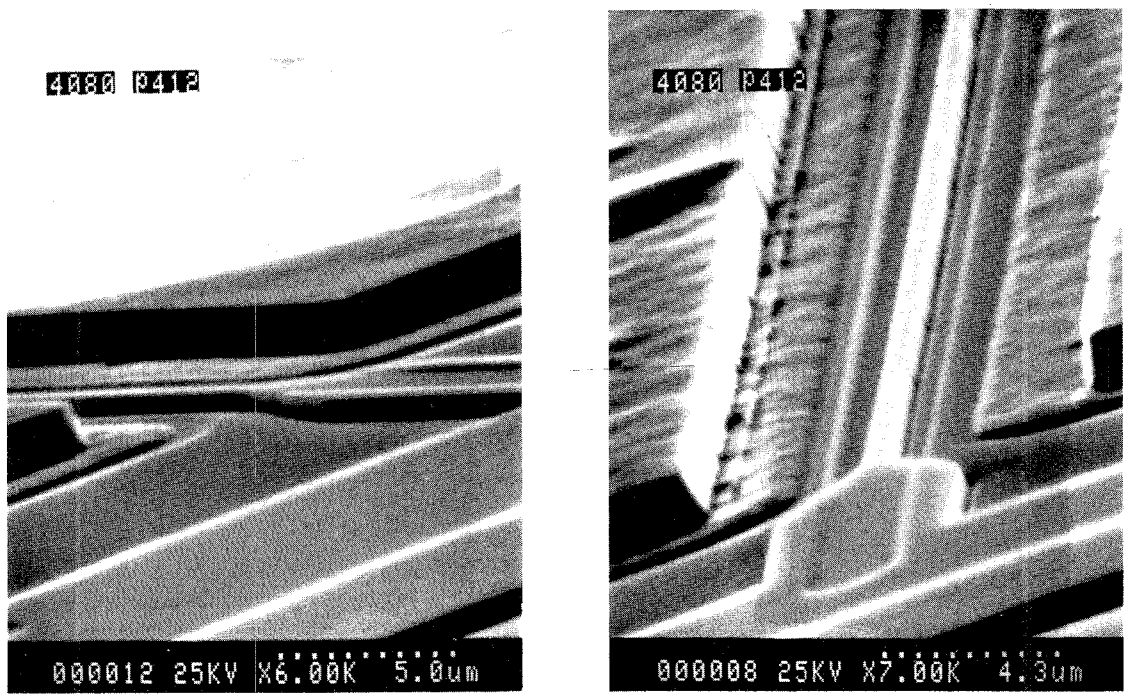

Figure 2 SEM photographs of a planar FET structure.

For devices fabricated on VPE or MBE materials, mesa etch is generally used to isolate the active devices. The mesa steps cause variations in the photoresist thickness which presents a major yield problem for submicron gate fabrication. In this work, a planar process is employed to eliminate the mesa by implanting the FET areas selectively using photoresist as the implant mask. The SEM photographs in Figure 2 illustrates the finished planar FET structure which greatly enhances the yield of the 0.8 um gates in the X-band power FETs.

POWER FET PERFORMANCE

X-band power FETs fabricated on the implanted materials have a typical I_{DSS} of 350 mA/mm and drain-source breakdown voltage (at pinchoff) in excess of 30 volts. Discrete FETs with 1 mm gate width have been power tested at 10 GHz. The output power and power added efficiency are plotted as functions of the input power in Figure 3. When biased at V_D = 10 volts, the output power at 1 dB compression is 760 mW with 7.5 dB gain and 36.5 percent power added efficiency. At V_D = 8 volts, a 40 percent power added efficiency has been measured from the same device with 720 mW output power and 6.3 dB gain. This combined high power and high efficiency matches the best MBE or VPE power FET performance.

MONOLITHIC POWER AMPLIFIER PERFORMANCE

The same planar, double-implantation process has been used to fabricate an X-band two-stage monolithic power amplifier. The amplifier design was reported in Reference 9. This amplifier chip (Figure 4), comprising

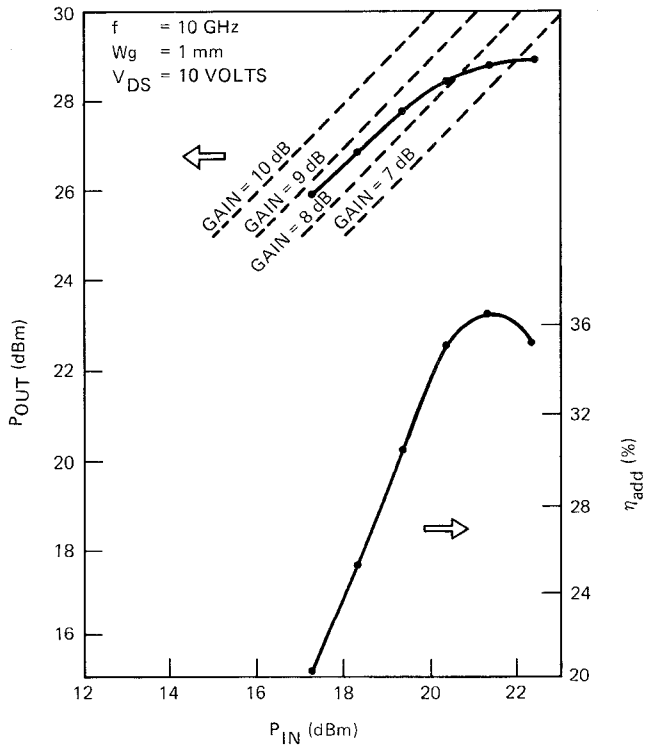

Figure 3 Output power and power added efficiency vs. input power measured at 10 GHz from a 0.8 um x 1 mm FET.

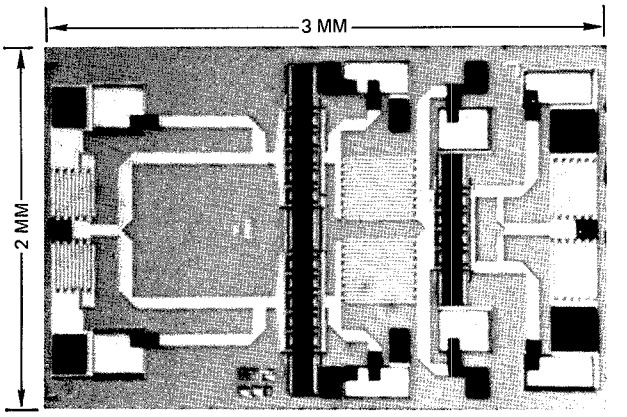

Figure 4 Photograph of a two-stage X-band monolithic power amplifier.

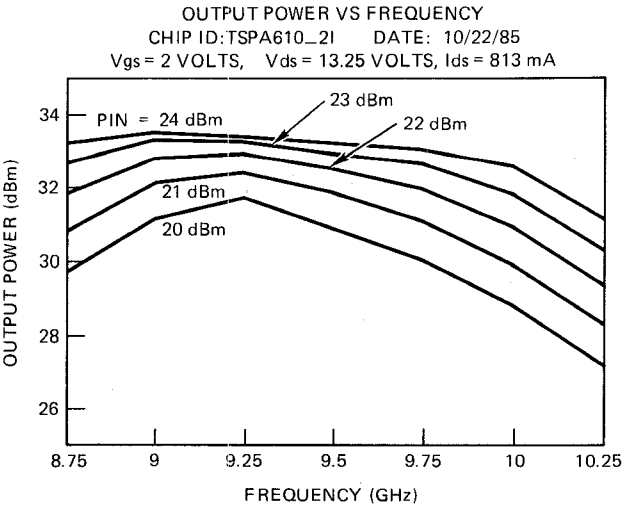

Figure 5 Output power vs frequency from a two-stage monolithic amplifier.

of a 0.8 um x 1.5 mm first-stage FET and a 0.8 um x 3.6 mm second-stage FET, was originally designed for VPE power FETs and did not provide optimum power matching to the newly developed implant FETs. Nevertheless, the monolithic amplifier still demonstrated a great improvement in performance. Figure 5 shows the amplifier output power, for several different input power levels, measured in the 8.75 to 10.25 GHz frequency range. The peak power at 9.5 GHz is 2.2 watts. This 0.6 W/mm power density represents a new record in the X-band monolithic power amplifier performance (see Reference 2 for comparison). This planar implantation process has also produced very good device yield and uniformity. DC yield of the monolithic power amplifier chip is better than 20 percent, and the standard deviation of I_{DSS} and V_{PO} (pinch-off voltage) are 4 percent and 5 percent, respectively.

CONCLUSION

Using an optimum double implantation profile and a planar process, high-yield, high-uniformity X-band power FETs and monolithic amplifiers have been fabricated and achieved a record 0.6 W/mm power density at 9.5 GHz. This process can be easily adapted for high volume, low cost production of high performance power MMICs.

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